MT9711

Programmable Hall Effect Linear Current Sensor IC

Bandwidth(250kHZ), UVD & OVD Detection, Wire Breakage Detection

MagnTek | Now Part of NOVOSENSE

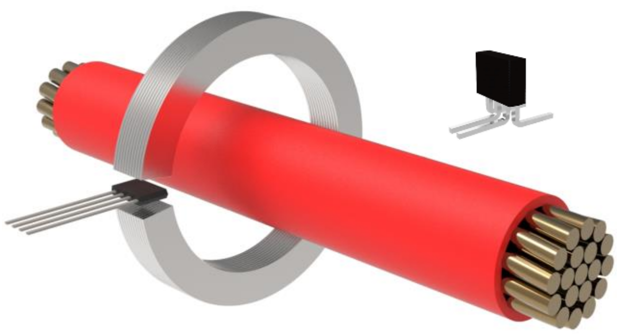
1 Product Description

The MagnTek® MT9711 product series is a programmable Hall effect linear sensor IC. The device can be used for accurate position sensing in a wide range of applications.

Each of the MT9711 consists of a highly sensitive Hall element, a low noise small-signal high-gain amplifier, a clamp and overcurrent protection output stage, and a high bandwidth dynamic offset cancellation technique.

The MT9711 provides an analog output voltage proportional to the applied magnetic flux density. The customer can configure the sensitivity and quiescent (zero field) output voltage through programming on the output pins, to optimize performance in the end application. The quiescent output voltage is user-adjustable around 50% of the supply voltage(VCC) and the output sensitivity is adjustable within the range of 0.5 to 6.5mV/G.

The MT9711 has voltage protection design, undervoltage detection, overvoltage detection and wire breakage detection, help end users design stable and reliable products.



2 Features

- AEC-Q100
- VCC ±20V withstand voltage protection
- VOUT +20V withstand voltage protection
- End-of-line programmable
- Sensitivity Programmed Range
  0.5~6.5mV/Gs
- High Bandwidth:
  --- 250kHz
- Wide Operating Temperature:
  --- -40℃~150℃
- Fast Output Response Time:
  --- 1.8μs
- Typical Accuracy:
  --- ±1.0% (25℃)
- High Linearity:
  --- ±0.5%
- High stability over operation temperature range:
  Sensitivity Drift:
  --- ±1.5% (-40℃~150℃)
  Quiescent Voltage Output Drift:
  --- ±5mV (-40℃~150℃)
- Diagnostic Detection :
  Undervoltage Detection
  Overvoltage Detection
  Wire breakage Detection
  Clamp Detection
- Package Option:
  --- SIP-4
  --- SIP-4, L-Bending
- Ratiometric Output
- RoHS Compliant: (EU)2015/863

3 Product Overview of MT9711A

Part Number	Sensitivity Range	Package	Packing
MT9711A-BAA-01	0.5~1.5 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9711A-BAA-2P5	1.5~3.5 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9711A-BAA-05	3.5~6.5 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9711A-KAA-01	0.5~1.5 mV/Gs	SIP-4	Tape & Reel (2000pcs/bag, 13 inch reel)
MT9711A-KAA-2P5	1.5~3.5 mV/Gs	SIP-4	Tape & Reel (2000pcs/bag, 13 inch reel)
MT9711A-KAA-05	3.5~6.5 mV/Gs	SIP-4	Tape & Reel (2000pcs/bag, 13 inch reel)
MT9711A-LAB-01	0.5~1.5 mV/Gs	SIP-4, L-Bending	Tape & Reel (500pcs/bag, 13 inch reel)
MT9711A-LAB-2P5	1.5~3.5 mV/Gs	SIP-4, L-Bending	Tape & Reel (500pcs/bag, 13 inch reel)
MT9711A-LAB-05	3.5~6.5 mV/Gs	SIP-4, L-Bending	Tape & Reel (500pcs/bag, 13 inch reel)

Table of Contents

Reversion History

1 Originally Version

4 Naming Specification

Part Number: MT9711 (❶) A (❷) - KA (❸) A (❹) - 01 (❺)

❶ Series Name

❷ Package Type

Type	Package
A	SIP-4

❹ Pin Height

Type	Pin Height
A	14.5mm
B	2.215mm

❸ Packing

Type	Packing
BA	SIP-4, Bulk packaging
KA	SIP-4, Tape & Reel
LA	L-Bending, Tape & Reel

❺ Sensitivity

Type	Sensitivity
01	1mV/Gs
2P5	2.5mV/Gs
05	5mV/Gs

5 Pin Configuration and Functions

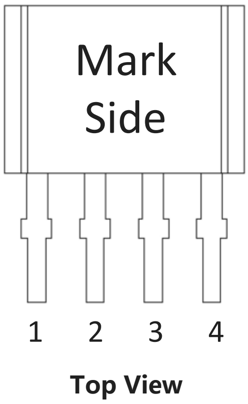


Figure.1 Pin Configuration & Functions

No.	Name	Description
1	VCC	Power Supply
2	VOUT	Analog Output Signal
3	NC	No Connect
4	GND	Signal Ground

6 Functional Block Diagram

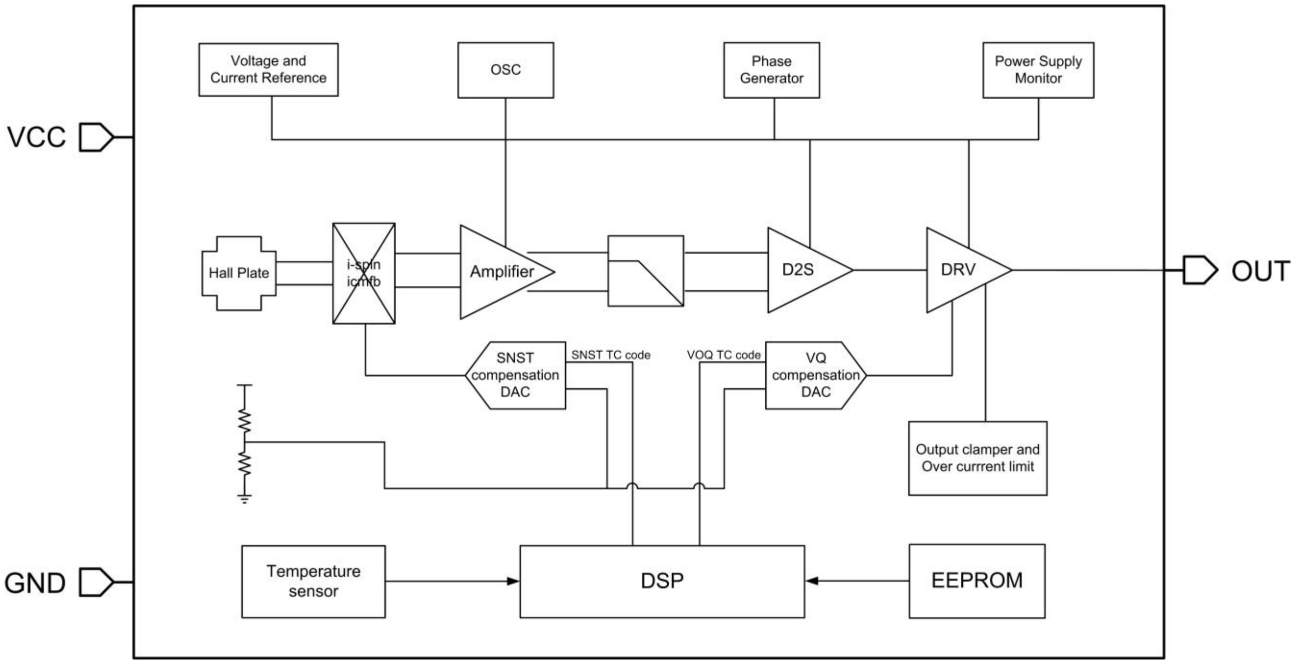


Figure.2 Functional Block Diagram

7 Typical Application Circuit

The typical application circuits of MT9711 series products include a bypass capacitor and a filter capacitor as an additional external components.
CBYPASS capacitor between VCC and GND is necessary, and it is recommended as 100nF.
CL capacitor between VOUT and GND is necessary, and it is recommended as 1nF.
Magnetic field applied vertically to the surface of the chip, the analog signal output is measured directly from the VOUT pin

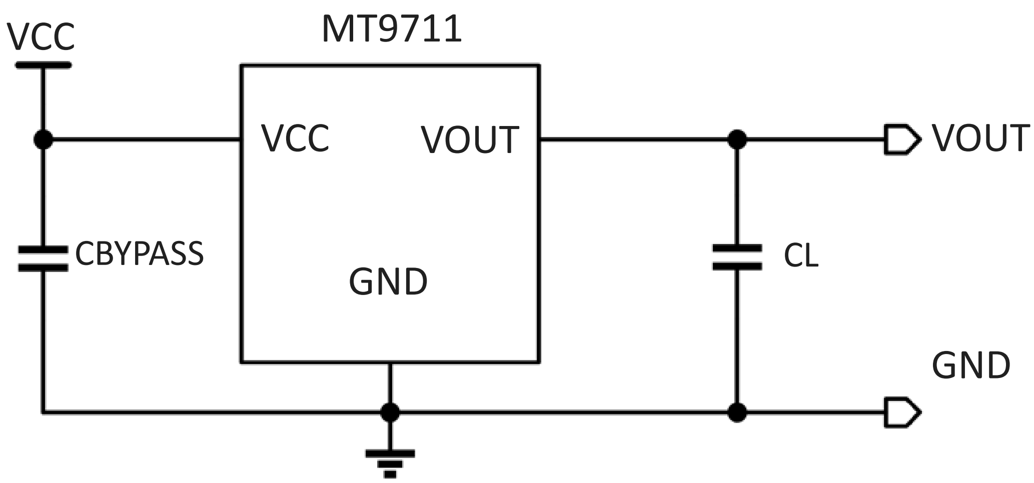


Figure.3 Typical Application Circuit

8 Electrical Magnetic Characteristics

8.1 Absolute Maximum Ratings

Absolute maximum ratings are limited values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Symbol	Parameters	Min	Max	Units
VCC	Supply Voltage	-	20	V
VRCC	Reverse Battery Voltage	-20	-	V
VOUT	Output Voltage	-	20	V
VROUT	Reverse Output Voltage	-0.5	-	V
IOUT(source)	Continuous Output Current(source)	-	40	mA
IOUT(sink)	Continuous Output Current(sink)	-	40	mA
TA	Operating Ambient Temperature	-40	150	℃
TS	Storage Temperature	-50	150	℃
TJ	Junction Temperature	-	165	℃
Endurance	Number of EEPROM Programming Cycles	-	1000	cycle

8.2 ESD Ratings

Symbol	Parametes	Reference	Values
VESD	Human-body model(HBM)	AEC-Q100-002	Class 3B
	Charged-device model(CDM)	AEC-Q100-011	Class C3
	Latch up（Latch up）	AEC-Q100-004	Class IIA

8.3 Electrical Specifications

T_A=-40~150 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
VCC	Supply Voltage	-	4.5	5	5.5	V
ICC	Supply Current	TA=25°C	-	9	15	mA
BW	Internal Bandwidth	TA=25℃	-	250	-	KHz
TRESP	Response Time	TA=25°C	-	1.8	-	us
TR	Rise time	TA=25°C	-	1.5	-	us
TPD	Propagation Delay	TA=25°C	-	1	-	us
VOL	Analog Output Low Saturation Level	RL>=4.7KΩ, TA=25°C	-	-	0.2	V
VOH	Analog Output High Saturation Level	RL>=4.7KΩ, TA=25℃	VCC-0.2	-	-	V
CL	Output Cap Load	OUT to GND	-	1	10	nF
RL	Output Res Load	Pull-down to GND	4.7	-	-	KΩ
		Pull-up to VCC	4.7	-	-	KΩ
ROUT	DC Output resistance	TA=25°C	-	5	-	Ω
IND	Noise Density	Input-referenced noise density; TA=25°C		1.2		mG/√Hz

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8.3 Electrical Specifications

T_A=-40~150 °C, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
TPO	Power on time	TA=25°C, no CBYPASS, CL=1nF	-	1	-	ms
VUVDH	Undervoltage Detection(UVD) High Voltage	TA=25°C, VCC rising	-	4.1	-	V
VUVDL	Undervoltage Detection(UVD) Low Voltage	TA=25°C, VCC falling	-	3.9	-	V
VUVDHYS	UVD Hysteresis	TA=25°C	-	0.2	-	V
TUVDR	UVD Delay Time	TA=25°C	-	2.2	-	us
VOVDH	Overvoltage Detection(OVD) High Voltage	TA=25°C, VCC rising	-	6.5	-	V
VOVDL	Overvoltage Detection(OVD) Low Voltage	TA=25°C, VCC falling	-	6.2	-	V
VOVDHYS	OVD Hysteresis	TA=25°C	-	0.3	-	V
TOVDR	OVD Delay Time	TA=25°C	-	1.2	-	us
VPORH	Power-On Reset High Voltage	TA=25°C, VCC rising	-	2.45	-	V
VPORL	Power-On Reset Low Voltage	TA=25°C, VCC falling	-	1.85	-	V
VPORHYS	Power-On Reset Hysteresis	TA=25°C	-	0.6	-	V
VBRK_H	Wire breakage Detection High Voltage	TA=25°C, RL=4.7KΩ to VCC, CL=1nF, refer to Figure.11	-	4.9	-	V
VBRK_L	Wire breakage Detection Low Voltage	TA=25°C, RL=4.7KΩ to GND, CL=1nF, refer to Figure.11	-	100	-	mV
ISCLP	Source Current of Over-Current-Limit	-	-	40	-	mA
ISCLN	Sink Current of Over-Current-Limit	-	-	40	-	mA
TSCLD	Detect Time for over-Current-Limit	TA=25°C	-	30	-	us
TSCLR	Release Time for over-Current-Limit	TA=25°C, IOUT>ISCLP or IOUT<ISCLN	-	1	-	ms
VCLP_LO	Clamp Low Output Level	TA=25℃, RL=10kΩ to VCC	0.25	-	0.35	V
VCLP_HI	Clamp High Output Level	TA=25℃, RL=10kΩ to GND	4.65	-	4.75	V
TCLP	Clamp Low Output Level	TA=25°C, magnetic field change from: 800 to 1200Gs, CL=1nF, SNST=2.5 mV/Gs	-	8	-	us

8.4 Accuracy Specification

T_A=-40~150 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters		Test Condition	Min	Typ	Max	Unit
ELIN	Nonlinearity Sensitivity Error		TA=25°C, VCC=5V	-0.5	-	0.5	%
VOQ	Quiescent Voltage Output		TA=25°C, VCC=5V, B=0Gs		0.5*VCC		V
VOE	Quiescent Voltage Output Error		TA=25°C, VCC=5V, B=0Gs	-5	-	5	mV
SNST_INIT	Initial Unprogrammed Sensitivity	01	TA=25°C, VCC=5V	0.988	1.000	1.012	mV/Gs
		2P5		2.470	2.500	2.530	mV/Gs
		05		3.940	5.000	5.060	mV/Gs
ERAT_SNST	Ratiometry Sensitivity Error		VCC=4.5 ~ 5.5 V, TA=25°C	-	±1.5	-	%
ERAT_VOQ	Ratiometry Quiescent Voltage Output Error		VCC=4.5 ~ 5.5 V, TA=25°C	-	±1	-	%
ERAT_CLP	Ratiometry Clamp Error		VCC=4.5 ~ 5.5 V, TA=25°C	-	±1	-	%
Programming Specification							
VOQ_STEP	Average Quiescent Voltage Output Programming Step Size		TA=25°C, VCC=5V	-	±1.25	-	mV
EVOQ_STEP	Quiescent Voltage Output Programming Resolution		TA=25°C, VCC=5V	-	±0.625	-	mV
SNST_PR	Sensitivity Programmed Range	01	TA=25°C, VCC=5V	0.5	-	1.5	mV/Gs
		2P5		1.5	-	3.5	mV/Gs
		05		3.5	-	6.5	mV/Gs
SNST_STEP	Average Sensitivity Programming Step Size		TA=25°C, VCC=5V	-	±0.3125	-	%
ESNST_STEP	Sensitivity Programming Resolution		TA=25°C, VCC=5V	-	±0.1562	-	%
Factory Temperature Coefficient Programed Specification							
ΔSNST_TC	Sensitivity Drift Through Temperature Range		TA=25°C to 150°C	-1.5	±0.8	1.5	%
			TA=–40°C to 25°C	-1.5	±0.8	1.5	%
ΔVOQ_TC	Quiescent Voltage Output Drift Through Temperature Range		TA=25°C to 150°C	-5	-	5	mV
			TA=–40°C to 25°C	-5	-	5	mV
Lock Bit Programming							
EELOCK_BIT	EEPROM Lock Bit			-	1	-	bit

9 Characteristic Definitions

Power On Time---TPO

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

The Power-On Time (TPO) is defined as the time taken between the supply reaching the minimum operating voltage VCCmin (t1), and the output voltage to settling to within ±10% of its steady state value under an applied magnetic field (t2) (See Figure 4).

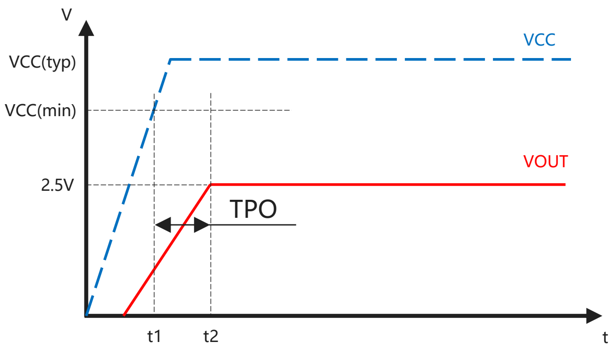


Figure.4 **Power On Time Definition**

Rise Time---TR

Rise Time is the time interval between the sensor VOUT reaching 10% of its full scale value (t1), and it reaching 90% of its full scale value (t2). (see Figure 6). Both TR and TRESP can be negatively affected by any eddy current losses created if a conductive ground plane is used.

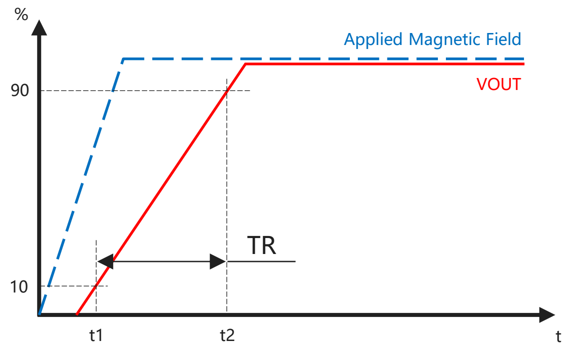


Figure.6 **Rise Time Definition**

Propagation Delay---TPD

The time interval between t1 when the primary current signal reaches 20% of its final value, and t2 when the output reaches 20% of its final value (see Figure 5).

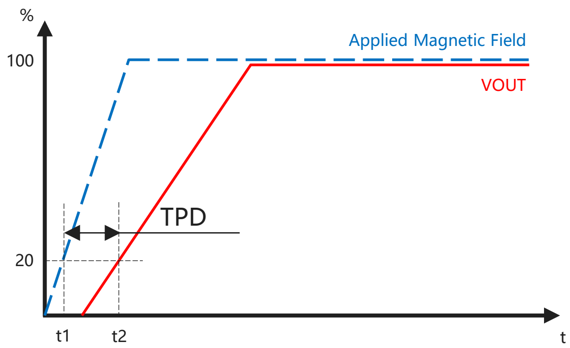


Figure.5 **Propagation Delay Definition**

Response Time---TRESP

The time interval between t1 when the primary current signal reaches 90% of its final value, and t2 when the sensor reaches 90% of its output corresponding to the applied current. (see Figure 7). Both TR and TRESP can be negatively affected by any eddy current losses created if a conductive ground plane is used.

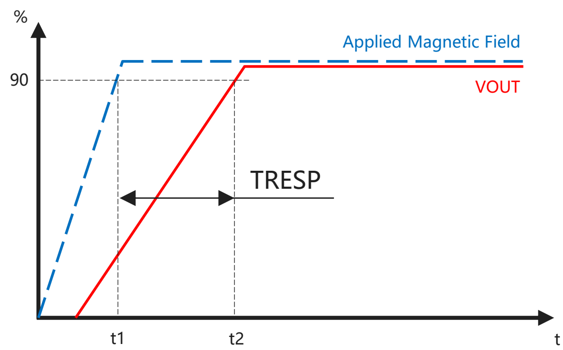


Figure.7 **Response Time Definition**

Delay to Clamp---TCLP

A large magnetic input step may cause the clamp to overshoot its steady state value. The Delay to Clamp (TCLP) is defined as the time it takes for the output voltage to settle within ±1% of its steady state value, after initially passing through its steady state voltage (see Figure 8) 。

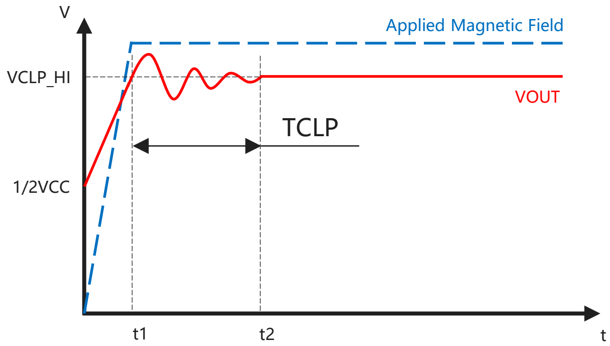


Figure.8 **Propagation Delay Definition**

Quiescent Voltage Output---VOQ

In the quiescent state (no significant magnetic field: B = 0GS), the output (VOQ), has a constant ratio to the supply voltage (VCC), throughout the entire operating ranges of VCC and ambient temperature (TA), VOQ=0.5*VCC。

Quiescent Voltage Output Drift Through Temperature Range---ΔVOQ_TC

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output (VOQ), may drift from its nominal value through the operating ambient temperature (TA). The Quiescent Voltage Output Drift Through Temperature Range, ∆ VOQ_TC, is defined as:

$$\Delta VOQ\_TC = VOQ(TA) - VOQ\_EXPECT(TA)$$

VOQ_TC should be calculated using the actual measured values of VOQ(TA) and VOQ_EXPECT(TA) rather than programming target values

Sensitivity---SNST

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.
Conversely, the application of a north polarity field decrease the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity(Sens(mV/G)),of the device, and it is defined as:

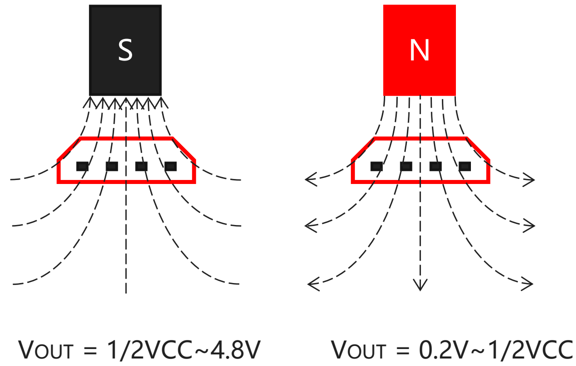


Figure.9 **Flux Direction Polarity**

$$SNST = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity Drift Through Temperature Range---ΔSNST_TC

Second order sensitivity temperance coefficient effects cause the magnetic sensitivity, to drift from its expected value over the operating ambient temperance range (TA). The Sensitivity Drift Through Temperature Range, ∆ SNST_TC, is defined as:

$$\Delta SNST\_TC = \frac{SNST(TA) - SNST\_EXPECT(TA)}{SNST\_EXPECT(TA)} * 100\%$$

Nonlinearity Sensitivity Error---ELIN

Ideally input magnetic field vs sensor output function is a straight line. The non-linearity is an indication of the worst deviation from this straight line. The ELIN in % is defined as:

$$ELIN = \left(\frac{SNST\_B1}{SNST\_B2} - 1\right) * 100\%$$

Where:

$$SNST\_B1 = \left(\frac{VOUT\_BPOS1 - VOUT\_BNEG1}{BPOS1 - BNEG1}\right)$$

$$SNST\_B2 = \left(\frac{VOUT\_BPOS2 - VOUT\_BNEG2}{BPOS2 - BNEG2}\right)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = |BNEG2| = Bmax, and |BPOS2| = 2 * |BPOS1| and |BNEG2| = 2 * |BNEG1|.

Ratiometry Error---ERAT

The MT9711 device features ratiometric output. This means that the Quiescent Voltage Output (VOQ), magnetic sensitivity (SNST) and Output Voltage Clamp (VCLP_HI, VCLP_LO), are proportional to the Supply Voltage (VCC). In other words, when the VCC increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the VCC relative to 5V, and the measured change in each Characteristic

Ratiometry Quiescent Voltage Output Error---ERAT_VOQ

ERAT_VOQ, for a given supply voltage, is defined as：

$$ERAT\_VOQ=\left(\frac{VOQ(VCC)/VCC}{VOQ(5V)/5V}-1\right)*100\%$$

Ratiometry Sensitivity Error--ERAT_SNST

ERAT_SNST, for a given supply voltage, is defined as：

$$ERAT\_SNST=\left(\frac{SNST\_B1(VCC)/VCC}{SNST\_B1(5V)/5V}-1\right)*100\%$$

Ratiometry Clamp Error---ERAT_CLP

ERAT_CLP, for a given supply voltage, is defined as:

$$ERAT\_CLP=\left(\frac{VCLP(VCC)/VCC}{VCLP(5V)/5V}-1\right)*100\%$$

Where VCLP is either VCLP_HI or VCLP_LO.

Over Current Limit---ISCLP & ISCLN

The MT9711 has over current protection function. When IOUT≥ISCLP or ISCLN, the output driver will be closed and the output will be turned into high resistance state.

Power-On Reset---POR, Undervoltage Detection---UVD, Overvoltage Detection---OVD

The descriptions in this section assume temperature = 25°C, no output load (RL, CL) , and no significant magnetic field is present.

Vcc Trend Up: During power-up, at initial stage, the output is in a high-impedance state, until the Vcc exceeds to VPORH, then the output of the chip will follow the Vcc. When the Vcc exceeds to VUVDH, the chip will enters the handshake protocol state firstly (~400uS), then chip goes to normal working state (Output=1/2*Vcc). When Vcc keeps trending up, and exceeds VOVDH, the output is in a high-impedance state.

Vcc Trend Down: If VCC drops below VOVDL, the output will back to normal working state (Output=1/2*Vcc). If Vcc keeps trending down, and below VUVDL, the output will follow the Vcc. If Vcc drops below VPORL, the output will be in a high-impedance state. (See Figure. 10).

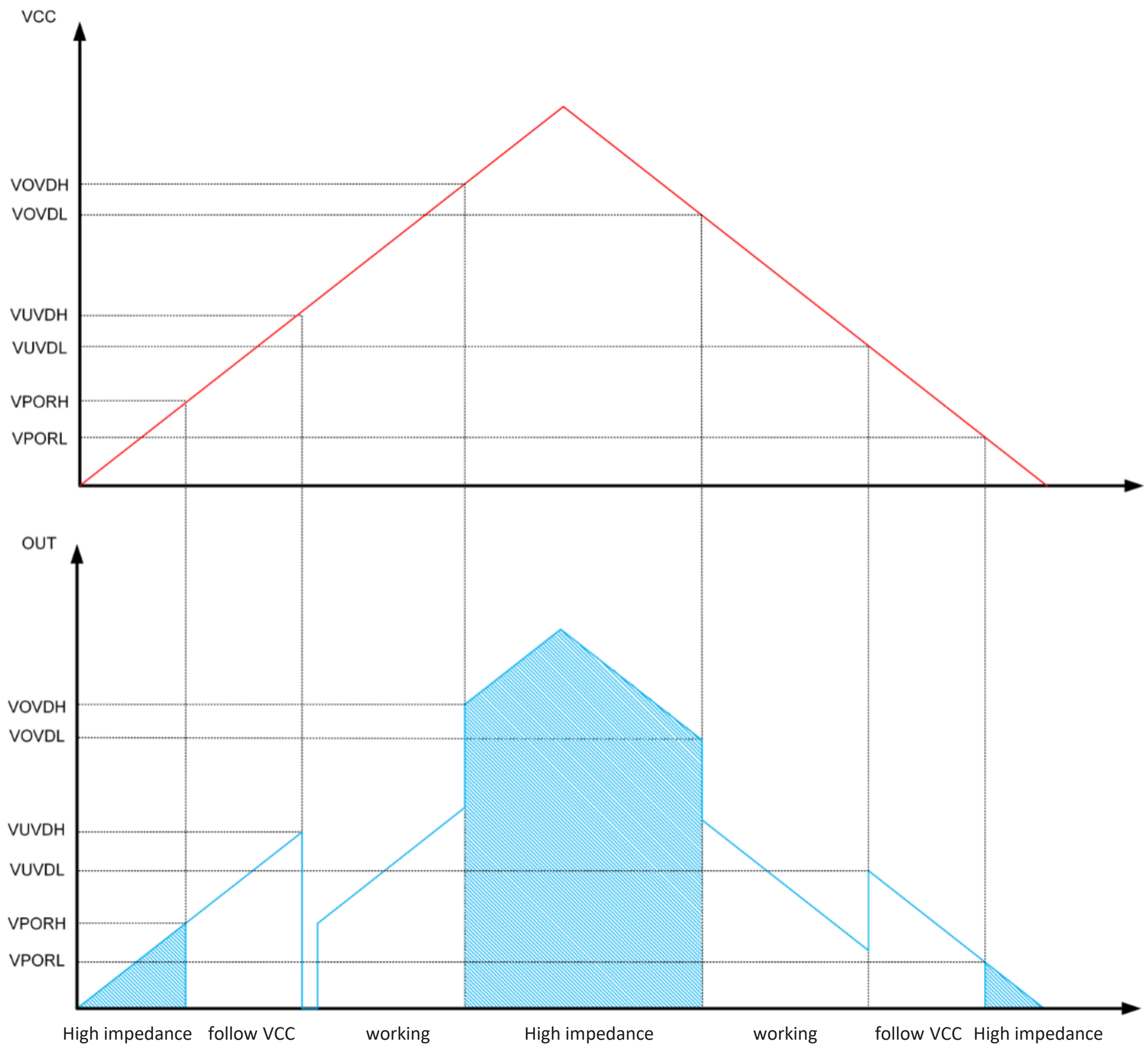


Figure.10 **POR 、UVD and OVD Definition**

Wire breakage Detection Voltage---VBRK

If the VCC 、 OUT or GND pins are disconnected (Wire breakage event), the output voltage will become VBRK_H (RL pull up to VCC) or VBRK_L (RL pull down to VCC)
CBYPASS capacitor between VCC and GND is necessary.

Statuc	RL	Wire breakage	VBRK
Power on	Pull up to VCC	VCC	High (VBRK_H)
		OUT	
		GND	
Working		VCC	
		OUT	
		GND	
Power on	Pull down to GND	VCC	LOW (VBRK_L)
		OUT	
		GND	
Working		VCC	
		OUT	
		GND	

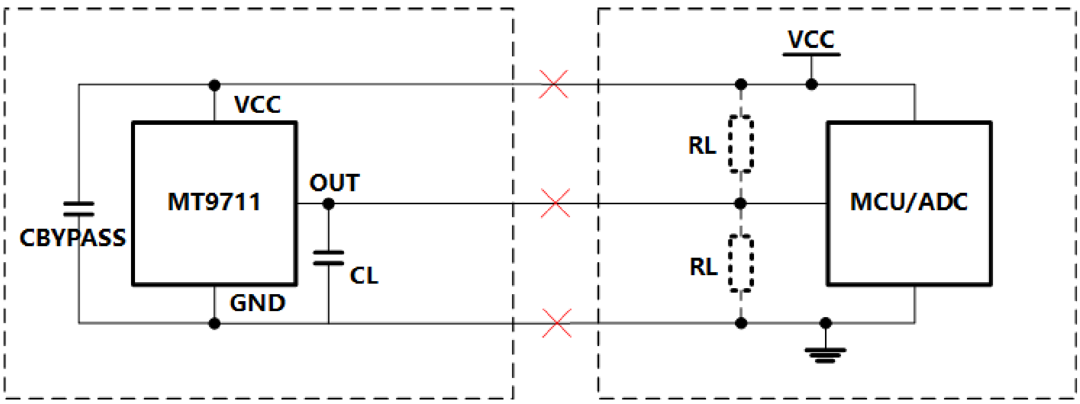
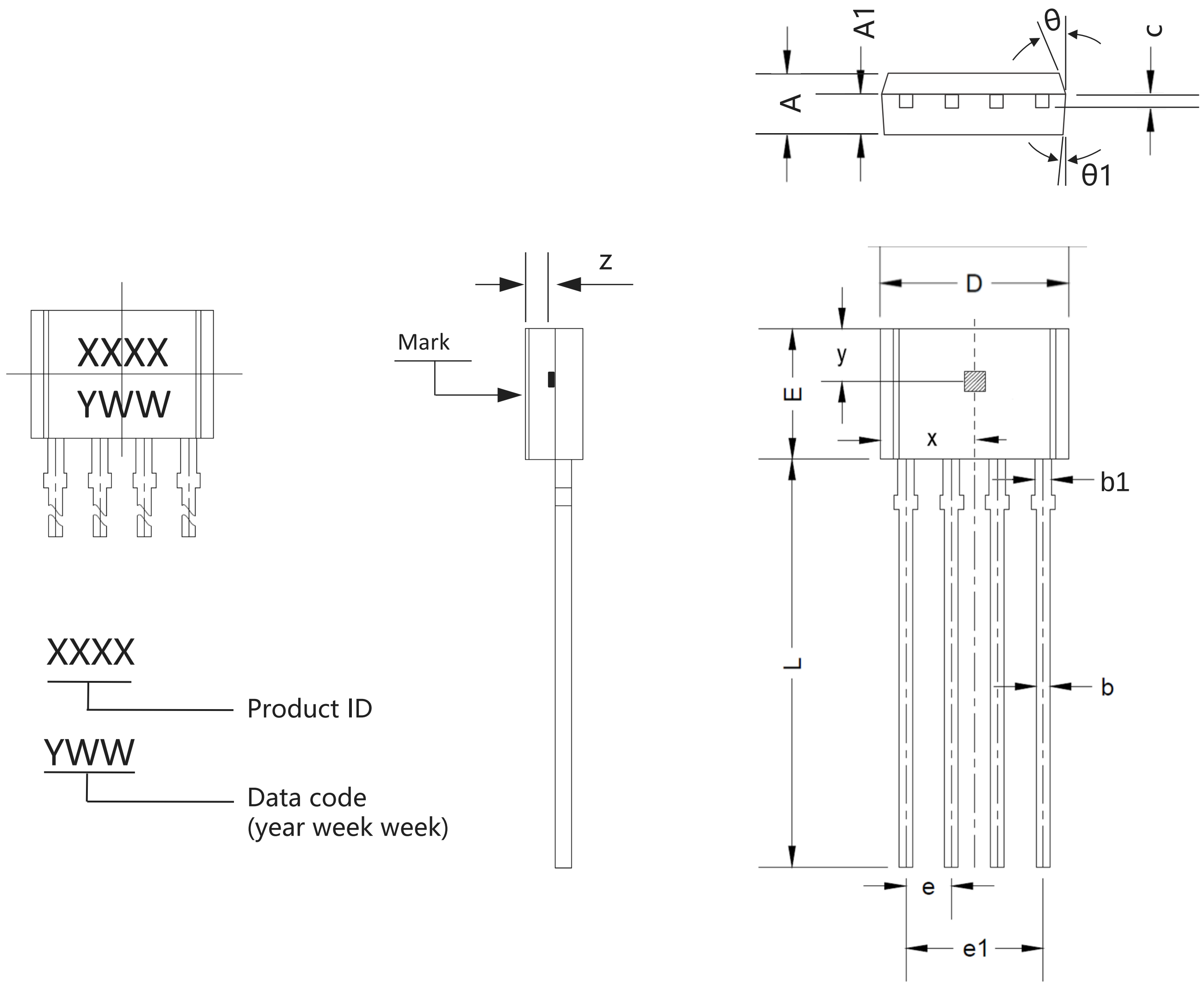


Figure.11 **VBRK Definition**

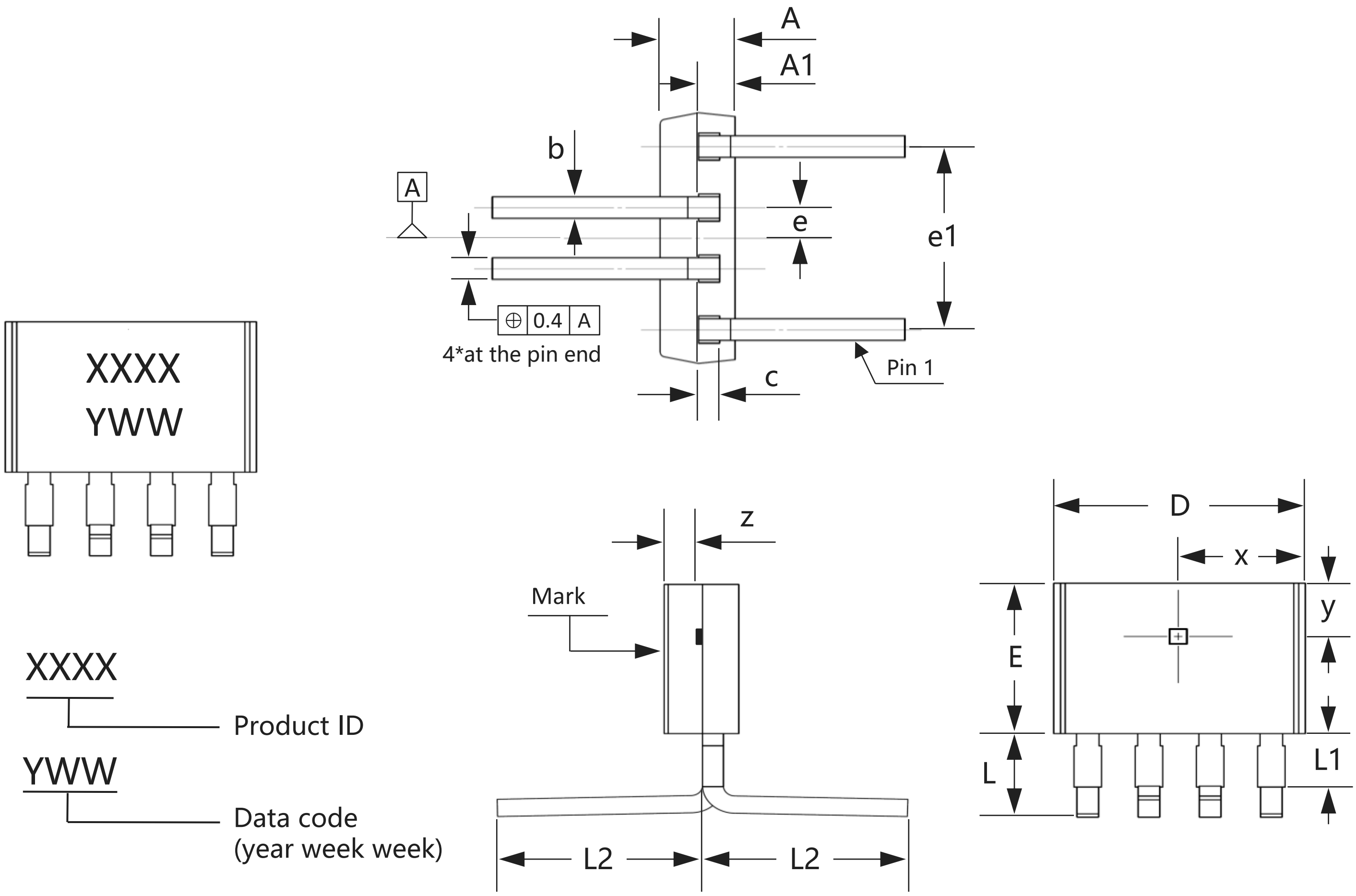
10 Package Material Information (For Reference Only – Not for Tooling Use)

10.1 SIP-4 Package Information (MT9711A-BAA/KAA-XX)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.460	1.660	0.057	0.065
A1	0.660	0.860	0.026	0.034
b	0.350	0.560	0.014	0.022
b1	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	5.120	5.320	0.202	0.209
E	3.550	3.750	0.140	0.148
e	1.270(BSC)		0.050(BSC)	
e1	3.810(BSC)		0.150(BSC)	
L	13.500	15.500	0.531	0.610
x	2.565(BSC)		0.101(BSC)	
y	1.545(BSC)		0.061(BSC)	
z	0.480(BSC)		0.019(BSC)	
Θ	11°		11°	
Θ1	6°		6°	

10.2 SIP-4, L-Bending Package Information (MT9711A-LAB-XX)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.460	1.660	0.057	0.065
A1	0.660	0.860	0.026	0.034
b	0.350	0.560	0.014	0.022
b1	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	5.120	5.320	0.202	0.209
E	3.550	3.750	0.140	0.148
e	1.270(BSC)		0.050(BSC)	
e1	3.810(BSC)		0.150(BSC)	
L	2.015	2.415	0.079	0.095
L1	1.3(BSC)		0.051(BSC)	
L2	4.100	4.500	0.161	0.177
x	2.565(BSC)		0.101(BSC)	
y	1.545(BSC)		0.061(BSC)	
z	0.480(BSC)		0.019(BSC)	

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